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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/708,788	03/25/2004	Joseph O. Marsh	FIS920030349US1	2787

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EXAMINER	
VELEZ, ROBERTO	

ART UNIT	PAPER NUMBER
2829	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/708,788	MARSH ET AL.	
	Examiner	Art Unit	
	Roberto Velez	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 February 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *16-19* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,6 and 20* is/are rejected.

7)☒ Claim(s) *3-5 and 7-15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 June 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *03/25/2004,04/06/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Claims 16-19 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 02/06/2008.

2. Applicant's election without traverse of invention I in the reply filed on 02/06/2008 is acknowledged.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gist et al. (US Pat. 5,657,456).

Regarding claim 1, Gist et al. shows (Figures 2-20) a circuit, comprising: a control circuit (not shown, but represented by signals 41 as disclosed col. 5, lines 9-15) adapted to generate at least a first and second signal (any of 40a-40g); a differential driver circuit [70] coupled to said control circuit (not shown, but represented by signals 41 as disclosed col. 5, lines 9-15), having a differential input node (any of 40a-40d) and a differential output node (connected to 30a) and adapted to receive a differential input signal at said differential input node, amplify said differential input signal and transmit a differential output signal onto said differential output node in response said first signal

(Col. 5, Ln 42-45 and Col. 16, Ln 51-60); a programmable termination impedance circuit [42] coupled to said control circuit (not shown, but represented by signals 41 as disclosed col. 5, lines 9-15) and said differential output node (connected to 30a), adapted to generate a differential termination impedance at said differential output node in response to said second signal (Col. 5, Ln 60-66); and a differential receiver circuit [90] coupled to said control circuit (not shown, but represented by signals 41 as disclosed col. 5, lines 9-15) and said differential output node (connected to 30a), adapted to receive (through connection to 30a) said differential output signal, convert (using 90b) said differential output signal to a single ended signal and transmit said single ended signal (Col. 21, Ln 35-57).

Gist et al. is silent about disclosing generating at least a first and second signal in response to a test enable signal and transmitting said single ended signal in response to said test enable signal.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to generating at least a first and second signal in response to a test enable signal and transmitting said single ended signal in response to said test enable signal. The ordinary artisan would have been motivated to modify Gist et al. in the manner set forth above for the purpose of saving energy by only having the control circuit and the differential receiver circuit activated when a test enable signal is received.

Note: It has been held that the recitation that an element is "adapted to" perform a function is not a positive limitation but only requires the ability to so perform. It does not constitute a limitation in any patentable sense. In re Hutchinson, 69 USPQ 138.

Regarding claim 20, Gist et al. shows (Figures 2-20) a circuit, comprising: means (not shown, but represented by signals 41 as disclosed col. 5, lines 9-15) for generating at least a first and second signal (any of 40a-40g); means [70] for receiving a differential input signal (any of 40a-40d), amplifying said differential input signal and transmitting a differential output signal onto a differential output node (connection to 30a) in response to said differential input signal and said first signal (Col. 5, Ln 30-45 and Col. 16, Ln 51-60); means [42] for generating a differential termination impedance at said differential output node in response to said second signal (Col. 5, Ln 60-66); and means [90] for receiving (through connection to 30a) said differential output signal, converting (using 90b) said differential output signal to a single ended signal and transmitting said single ended signal (Col. 21, Ln 35-57).

Gist et al. is silent about disclosing generating at least a first and second signal in response to a test enable signal and transmitting said single ended signal in response to said test enable signal.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to generating at least a first and second signal in response to a test enable signal and transmitting said single ended signal in response to said test enable signal. The ordinary artisan would have been motivated to modify Gist et al. in the manner set forth above for the purpose of saving energy by only having the control

circuit and the differential receiver circuit activated when a test enable signal is received.

5. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gist et al. (US Pat. 5,657,456) in view of Barnhart (US Pat. 6,185,710).

Gist et al. discloses everything as claimed above in claim 1.

Gist et al. fails to disclose a first shift-register-latch circuit coupled to said differential input node and adapted to store said differential input signal; and a second shift-register-latch circuit coupled to said differential receiver circuit and adapted to store said transmitted single ended signal. However, Barnhart shows (Fig. 2) a first shift-register-latch circuit [64] coupled to said differential input node (connection to 80) and a second shift-register-latch circuit [64] coupled to said differential receiver circuit [82].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Barnhart into the device of Gist et al. by including a first shift-register-latch circuit coupled to said differential input node and adapted to store said differential input signal; and a second shift-register-latch circuit coupled to said differential receiver circuit and adapted to store said transmitted single ended signal. The ordinary artisan would have been motivated to modify Gist et al. in the manner set forth above for the purpose of being able to apply different testing signals at different time periods with high quality performance.

Note: It has been held that the recitation that an element is "adapted to" perform a function is not a positive limitation but only requires the ability to so perform. It does not constitute a limitation in any patentable sense. In re Hutchinson, 69 USPQ 138.

6. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gist et al. (US Pat. 5,657,456) in view of Tobin et al. (US Pat. 6,535,945).

Gist et al. discloses everything as claimed above in claim 1.

Gist et al. fails to disclose wherein said programmable termination impedance circuit comprises a plurality of resistor components, each resistor component having an associated switch for selectively connecting that resistor component from a voltage source to said differential output node. However, Tobin et al. shows (Fig. 8) wherein said programmable termination impedance circuit [810] comprises a plurality of resistor components [R_1-R_4], each resistor component [R_1-R_4] having an associated switch [Q_1-Q_4] for selectively connecting that resistor component [R_1-R_4] from a voltage source (V_{OUT} Or V_{dd}) (Col. 10, Ln 55-65).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Tobin et al. into the device of Gist et al. by including in the programmable termination impedance circuit comprises a plurality of resistor components, each resistor component having an associated switch for selectively connecting that resistor component from a voltage source to said differential output node. The ordinary artisan would have been motivated to modify Gist et al. in the manner set forth above for the purpose of varying the resistance of the circuit depending on the desired degree or range of resistance control.

Allowable Subject Matter

7. Claims 20-21, 25-27, 34-35 and 37 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. The following is a statement of reasons for the indication of allowable subject manner: the prior art of record, taken alone or in combination, fails to disclose or render obvious, a circuit comprising: a differential driver circuit, wherein the differential driver circuit comprises: a plurality of FIR latches coupled to said differential input node and adapted to store said differential input signal; a plurality of preamplifier circuits coupled to said FIR latches and adapted to amplify said differential input signal, wherein said preamplifier circuits are enabled in response to said first signal; a driver output stage coupled to said preamplifier circuits and adapted to transmit said differential output signal; and a current DAC circuit coupled to said driver output stage and adapted to set drive strength of said driver output stage in response to a plurality of IDAC control signals, as further recited in claim 3;

a circuit comprising: a programmable termination impedance circuit comprising a plurality of resistors, wherein at least one, but less than all of said resistor components are coupled to a first node of said differential output node and a remainder of said resistor components are coupled to a second node of said differential output node, as further recited in claim 7;

a circuit comprising: a differential receiver circuit comprising: a differential amplifier circuit coupled to said differential output node and adapted to receive said

differential output signal; a built-in offset voltage comparator circuit coupled to said differential amplifier circuit and adapted to output a signal in response to said differential output signal and an offset voltage; an output stage coupled to said differential amplifier circuit and said built-in offset voltage comparator circuit and adapted to transmit said single ended signal in response to said output signal of said built-in offset volt\- age comparator circuit; and a level shifter circuit coupled to said output stage and adapted to transition power supply domains from an analog power supply domain to a digital power supply domain, as further recited in claim 11.

Claims 4-5, 8-10 and 12-15 depending from claims 3, 7 or 11 are objected for the same reason.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Coyle et al. (US Pat. 6,609,221) discloses a method and apparatus for inducing bus saturation during operational testing of busses using a pattern generator.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Roberto Velez whose telephone number is 571-272-8597. The examiner can normally be reached on Monday-Friday 8:00am- 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ha Nguyen can be reached on 571-272-1678. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Roberto Velez/
Examiner, Art Unit 2829
04/21/2008

/Ha T. Nguyen/
Supervisory Patent Examiner, Art Unit 2829